1. A method of forming an isolation region in a semiconductor substrate, comprising the steps of:

forming an insulator filled shallow trench shape with a smooth top surface topography in a first portion of said semiconductor substrate;

forming a deep trench shape in said insulator filled shallow trench shape and in an underlying second portion of said semiconductor substrate;

forming an insulator layer on exposed semiconductor surfaces of said deep trench shape;

forming a conductive shape in bottom portion of said deep trench shape; and

forming an insulator plug with a smooth top surface topography in a top portion of said deep trench shape overlying conductive shape, resulting in said isolation region comprised with said deep trench shape, featuring said insulator plug on underlying said conductive shape, with a top portion of said deep trench shape surrounded by said insulator filled shallow trench shape.

2. The method of claim 1, wherein an opening used to define said insulator filled shallow trench shape is formed in a silicon nitride layer comprised with a thickness between 1100 to 2000 Angstroms.

3. The method of claim 1, wherein depth of shallow trench shape of said insulator filled shallow trench shape, in said top portion of said semiconductor substrate, is between about 3000 to 5000 Angstroms.

4. The method of claim 1, wherein insulator layer used for said insulator filled shallow trench shape is a silicon oxide layer, having a thickness between about 8000 to 10,000 Angstroms.

5. The method of claim 1, wherein a planarization procedure used to create a smooth top surface topography for said insulator filled shallow trench shape, is a chemical mechanical polishing (CMP), procedure.

6. The method of claim 1, wherein said deep trench shape is formed via an anisotropic reactive ion etching (RIE), procedure, using CHF_3 as an etchant for insulator layer in said insulator filled shallow trench shape, and using Cl_2 as an etchant for silicon in said second portion of said semiconductor substrate.

7. The method of claim 1, wherein the depth of said deep trench shape in said second portion of said semiconductor substrate, is between about 4 to 10 um.

8. The method of claim 1, wherein the diameter of said deep trench shape is between about 0.5 to 1.6 um.

9. The method of claim 1, wherein said insulator layer formed on the sides of said semiconductor substrate in said deep trench shape, is a silicon dioxide layer, obtained via thermal oxidation procedures to a thickness between about 50 to 1000 Angstroms.

10. The method of claim 1, wherein a region located in a third portion of said semiconductor substrate, directly underlying bottom of said deep trench shape, is a P type channel stop region, obtained via implantation of boron or BF_2 ions, at an energy between about 3 to 90 KeV, at a dose between about 1E12 to 1E15 atoms/cm^2, and using a zero degree implantation angle.

11. The method of claim 1, wherein said conductive shape, located in said bottom portion of said deep trench shape, is comprised of polysilicon.

12. The method of claim 1, wherein said conductive plug is recessed to a depth between about 1000 to 5000 Angstroms below the top surface of said insulator filled shallow trench shape, via a RIE procedure using Cl_2 as an etchant.

13. The method of claim 1, wherein said insulator plug located in a top portion of said deep trench shape is comprised of silicon oxide, obtained via high density plasma deposition procedures.

14. The method of claim 1, wherein said insulator plug located in a top portion of said deep trench shape, is formed with a smooth top surface topography via subjection to a CMP procedure.

15. A method of forming a smooth top surface topography for an isolation region in a semiconductor substrate, wherein said isolation region is comprised of a shallow trench - deep trench configuration, comprising the steps of:

depositing a silicon nitride layer;

forming a shallow trench shape in said silicon nitride layer and in a first portion of said semiconductor substrate;

depositing a first silicon oxide layer completely filling said shallow trench shape;

performing a first chemical mechanical polishing (CMP), procedure to remove a top portion of said first silicon oxide layer, forming an insulator filled shallow trench shape with a smooth top surface topography;

forming a deep trench opening in said insulator filled shallow trench shape and in an underlying second portion of said semiconductor substrate;

growing a silicon dioxide layer on surface of portions of said semiconductor substrate exposed in said second portion of said deep trench opening;

performing an ion implantation procedure to form a channel stop region of the same dopant type as said semiconductor substrate, in a third portion of said semiconductor substrate, located underlying bottom of said deep trench opening, with the dopant concentration of said channel stop region greater than the dopant concentration of said semiconductor substrate;

depositing a second silicon oxide layer, not filling said deep trench opening;

depositing a polysilicon layer completely filling said deep trench opening;

removing portions of said polysilicon layer and exposed portions of said second silicon oxide layer, resulting in a recessed polysilicon shape in a bottom portion of said deep trench opening;

depositing a third silicon oxide layer completely filling a space in a top portion of said deep trench opening;

performing a dry etch procedure using a photoresist shape as a mask, to remove portions of said third silicon oxide layer and bottom portions of said first silicon oxide layer, from the top surface of said silicon nitride layer, resulting in an insulator stack comprised of said third silicon oxide layer and of a bottom portion of first silicon oxide layer, with said insulator stack overlying insulator filled shallow tench shape, and overlying adjacent portions of said silicon nitride layer;

performing a second CMP procedure to remove said insulator stack from the top surface of said adjacent silicon nitride layer resulting in a deep trench shape comprised of a third silicon oxide plug in a top portion of said deep trench opening, overlying said recessed polysilicon shape in turn located in said bottom portion of said deep trench opening, with top surface of said deep trench shape and said silicon nitride layer creating a smooth top surface topography; and

removing said silicon nitride layer.

16. The method of claim 15, wherein said silicon nitride layer is obtained via low pressure chemical vapor deposition (LPCVD), or plasma enhanced chemical vapor deposition (PECVD), procedures, at a thickness between about 1100 to 2000 Angstroms.

17. The method of claim 15, wherein depth of shallow trench shape in said top portion of said semiconductor substrate, is between about 3000 to 5000 Angstroms.

18. The method of claim 15, wherein first silicon oxide layer is obtained via LPCVD or PECVD procedures, at a thickness between about 8000 to 10000 Angstroms, using a high density plasma (HDP), deposition procedure, and using tetraethylorthosilicate (TEOS), as a source.

19. The method of claim 15, wherein the thickness of said first silicon oxide layer remaining on said silicon nitride layer after said first chemical mechanical polishing (CMP), procedure, is between about 1000 to 3000 Angstroms.

20.The method of claim 15, wherein the depth of said deep trench opening in said second portion of said semiconductor substrate, is between about 4 to 10 um.

21.The method of claim 15, wherein the diameter of said deep trench opening is between about 0.5 to 1.6 um.

22. The method of claim 15, wherein said silicon dioxide layer formed on the surfaces of said semiconductor substrate exposed in said deep trench opening, is obtained via thermal oxidation procedures at a thickness between about 50 to 1000 Angstroms.

23. The method of claim 15, wherein said second silicon oxide layer has a thickness between about 500 to 3000 Angstroms.

24. The method of claim 15, wherein said polysilicon layer is obtained via LPCVD procedures at a thickness between about 7,000 to 20,000 Angstroms.

25. The method of claim 15, wherein said recessed polysilicon shape is recessed to a depth between about 1000 to 5000 Angstroms below the top surface of said insulator filled shallow trench shape.

26. The method of claim 15, wherein said third silicon oxide layer has a thickness between about 1000 to 8000 Angstroms.

27. The method of claim 15, wherein said third silicon oxide plug is formed in said top portion of said deep trench shape, via said second chemical mechanical polishing procedure.

28. The method of claim 15, wherein said silicon nitride layer is selectively removed via wet etch procedures using a hot phosphoric acid solution.

29. A shallow trench - deep trench structure in a semiconductor substrate, comprising:

an insulator filled shallow trench shape located in a first portion of said semiconductor substrate;

a deep trench shape located in said insulator filled shallow trench shape, and extending into an underlying second portion of said semiconductor substrate;

a channel stop region located in a third portion of said semiconductor substrate, directly underlying bottom of said deep trench shape;

insulator sidewalls located on the sides of a bottom portion of said deep trench shape;

a conductive shape located in said bottom portion of said deep trench shape interfacing said insulator sidewalls; and

an insulator shape located in a top portion of said deep trench shape, overlying said conductive shape, with sides of said insulator shape interfacing insulator filled shallow trench shape.

30. The shallow trench - deep trench structure of claim 29, wherein the depth of said insulator filled shallow trench shape in said first portion of said semiconductor substrate is between about 1100 to 2000 Angstroms.

31.The shallow trench - deep trench structure of claim 29, wherein said insulator filled shallow trench shape is filled with silicon oxide.

32. The shallow trench - deep trench structure of claim 29, wherein the depth of said deep trench shape, in said first portion of said semiconductor substrate and in said second portion of said semiconductor substrate, is between about 4 to 10 um.

33. The shallow trench - deep trench structure of claim 29, wherein the diameter of said deep trench shape is between about 0.5 to 1.6 um.

34. The shallow trench - deep trench structure of claim 29, wherein said conductive shape, located in said bottom portion of said deep trench shape, is comprised of polysilicon.

35.The shallow trench - deep trench structure of claim 29, wherein said insulator shape, located in said top portion of said deep trench shape, is comprised of silicon oxide.